REMARKS

This Amendment amends claims 3-4 and adds new claims 18 and 19. Claims 1-19 are pending. Claims 1 and 3 are independent.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**" It is noted that the amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

The Office Action objects to claim 4. This Amendment amends claim 4 in accordance with Examiner Soward's helpful suggestion.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, is directed to a semiconductor device which includes a relatively low threshold level MOSFET and relatively high threshold level MOSFETs of n– and p- type. The high threshold level MOSFETs have gate oxide films which are thicker than that of the lower threshold level MOSFET. Additionally, the gate oxide film of the high threshold level n-type MOSFET is thicker than the gate oxide film of the high threshold level p-type MOSFET. Therefore, there are three different thicknesses of the gate oxide films. Implantation treatments of fluoride ions in the regions of the high threshold level MOSFETs are performed before forming the gate oxide films. Each implantation being different for the high threshold level MOSFETs.

This configuration provides a semiconductor structure which can achieve high speed operation, high reliability and low consumption power because suitable gate oxide film thicknesses are provided.

II. THE APPLIED REFERENCES

The Office Action rejects claims 1-17 under 35 U.S.C. § 103(a) over Shimizu et al. in view of Huang et al. Applicants respectfully traverse this rejection.

None of the applied references teaches or suggests the features of independent claims 1 and 3 including: 1) a third MOSFET of a p-type design . . . having a third gate oxide film which is thicker than the first gate oxide film and thinner than the second gate oxide film (claims 1 and 3); 2) selectively implanting fluorine ions in the first part of the second region (claim 3); and 3) selectively implanting fluorine ions into the second part of the second region (claim 3). Shimizu et al. discloses memory transistors with varying gate oxide thicknesses. Shimizu et al. discloses a first transistor A with a thin gate oxide film I_{t1} of 500 angstroms and a thick inter-layer oxide film I_{t2} of 1200 angstroms (col. 2, lines 49-53). The second transistor B includes the thin gate oxide film I_{t1} of 500 angstroms and the third transistor C includes a thick gate oxide film I_{t2} of 1000 angstroms (col. 2, lines 54-61). In other words, the gate oxide thicknesses of each of the transistors is 500 angstroms for transistors A and B and 1000 angstroms for transistor C. Thus, Shimizu et al. discloses only two different thicknesses of gate oxide films.

Applicants note that the Office Action incorrectly appears to assert that the layer I_{t2} of transistor A in Shimizu et al. is a gate oxide film. To the contrary, the layer I_{t2} of transistor A in

Shimizu et al. is an interlayer oxide layer (col. 2, lines 52-53). For the sake of argument, if the interlayer oxide layer I_{t2} of transistor was a gate oxide film, then the statement that the "second gate oxide film I_{t1} thicker (sic) than the first gate oxide film" cannot be true because the layer I_{t2} on transistor A is 1200 angstroms thick while the layer I_{t1} on transistor B is 500 angstroms thick. Similarly, the statement that the "third gate oxide film I_{t2} . . . is thicker than the first gate oxide film" is also incorrect because the third gate oxide film I_{t2} on transistor C is 500 angstroms which is thinner than the layer I_{t2} of transistor A which is 1200 angstroms.

Additionally, as pointed out by the Office Action, all of the transistors disclosed by Shimizu et al are n-type transistors. Shimizu et al. does not teach or suggest a third MOSFET of a p-type design . . . having a third gate oxide film which is thicker than the first gate oxide film and thinner than the second gate oxide film as recited in independent claims 1 and 3. Huang et al. does not remedy the deficiencies of Shimizu et al.

Huang et al. discloses a method for fabricating a dual-gate dielectric module for memory embedded logic. In particular, Huang et al. discloses n-type and p-type transistors in a logic region 12 of a semiconductor device. The gate thicknesses 20 for each of these transistors are identical and are disclosed as being between 20 and 200 angstroms (see Table of Elements and preferred parameter limits in col. 5 and col. 7, lines 51-53). Huang et al. discloses a second gate thickness 34 for use in a memory region 14 as ALSO being between 20 and 200 angstroms (see Table of Elements and preferred parameter limits in col. 5 and the table in col. 8). Huang et al. does not disclose transistors of different types being formed together on the same semiconductor device with each type of transistor having different gate thicknesses are recited in independent

claims 1 and 3.

Moreover, while both Shimizu et al. and Huang et al. appear to disclose two different gate thickness levels, none of the applied references teaches or suggests a third gate thickness level.

Lastly, none of the applied references teaches or suggests the features of independent claim 3 including selectively implanting fluorine ions in the first part of the second region and selectively implanting fluorine ions into the second part of the second region. Applicants respectfully request withdrawal of this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that the Application is in condition for allowance. Applicants respectfully request prompt reconsideration and allowance.

Should the Examiner believe that anything further is desirable to place the Application into condition for allowance, Applicants invite the Examiner to contact the undersigned attorney at the telephone number listed below.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 5/28/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Please amend claims 3-4 and add new claims 18- 19 as follows:

3. (Amended) A method for fabricating on a semiconductor substrate a semiconductor device [as claimed in claim 1], the method comprising:

forming an isolation region within [the] a semiconductor substrate and close to a surface of the semiconductor substrate to define a first region for [the] a first gate oxide film of a first MOSFET and a second region for [the] second and third MOSFETs;

selectively implanting fluorine ions into a first part of the second region with a first ion-implantation condition, the first part of the second region being for the second MOSFET, the first ion-implantation condition being determined to form [the] a second gate oxide film;

selectively implanting fluorine ions into a second part of the second region with a second ion-implantation condition, the second part of the second region being for the third MOSFET, the second ion-implantation condition being determined to form [the] a third gate oxide film;

simultaneously growing oxide films on and over the first and second regions of the semiconductor substrate; and

forming the first to third MOSFETs by using the simultaneously grown oxide films, so that the first to third MOSFETs have the first to third gate oxide films, respectively, wherein the second gate oxide film is thicker than the first gate oxide film and the third gate oxide film is thicker than the first gate oxide film and is thinner than the second gate oxide film; and

wherein the threshold level of the first MOSFET is relatively low and the threshold levels of the second and third MOSFETs are relatively high, and the second MOSFET is an n-type and the third MOSFET is a p-type.

4. (Amended) A fabrication method as claimed in claim 3. wherein the first and second ion-implantation conditions are determined so that the third gate oxide film is thinner than the second gate oxide film.

- - 18. (Newly Added) The method of claim 3. wherein the second and third MOSFETs have equal gate-channel leakage current characteristics. - -

- - 19. (Newly Added) The method of claim 18. wherein the standby current in each of the second and third MOSFETs do not depend on the gate-channel leakage current characterisics but on the subthreshold characteristics. - -